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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,099	09/09/2003	Chih-Hung Wang	11555-US-PA	2098

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
FARROKH, HASHEM	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,099	WANG, CHIH-HUNG	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-9* is/are rejected.

7)☒ Claim(s) *6 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the Applicant's Remarks dated November 1, 2005. The instant application having application No. 10/605,099 has a total of 9 claims pending in the application; claims 1-2, 4-5, and 9-10 have been amended; claim 3 has been canceled; no new claims have been added.

INFORMATION CONCERNING SPECIFICATION:

Specification

The disclosure is objected to because of the following informalities:

1. *The expression* "...each page has a plurality of sectors by N..." *in paragraph 14 of the specification is not a proper use of English language. It is suggested that the Applicant review the entire specification and make any correction deemed necessary.*

Appropriate correction is required.

INFORMATION CONCERNING CLAIMS:

Claim Objections

2. *Claim 2 is objected to because of the following informalities: The expression* "wherein the at least two buffer in the controller is buffers" *is incorrect.*

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> *The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

3. Claims 1-2 and 4-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The Applicant amendment has erased the word "flash" *in the expression* "flash memory" *in the claims. By doing so the Applicant have broadened the scope of invention to include any type of memory. The paragraph 2 of the specification states:* "The present invention relates to access operation for a large block flash memory. More particularly, the present invention relates to an access operation on a large block flash memory by a pipeline manner." *(Emphasis added). The Examiner has searched the specification and has not been able to find any support for this change. The Applicant is required to make an amendment to overcome these rejections.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims *1-2, 4-5, and 7-9* are rejected under 35 U.S.C. 103(a) as being unpatentable over *U.S. Patent No. 6871,257 B2 to Conley et al. (hereinafter Conley) in view of U.S. Patent No. 6,907,497 B2 to Hosono et al. (hereinafter Hosono).*

4. In regard to claim 1, Conley teaches:

"An accessing method to a large block memory **(e.g., see column 1, line 10, elements 131 in Fig. 2)** of a memory device, **(e.g., see column 1, lines 30-34)** wherein the large block flash memory has a plurality of pages **(e.g., see column 1, line 44)** and each page has a plurality of sectors, **(e.g., see column 1, line 46)** wherein the memory device has a controller to control an access operation between a host and the large block memory of the memory device, **(e.g., see column 3, lines 62-67; column 4, lines 1-1-4; elements 101 and 131 in Fig. 2)** wherein the controller includes at least two buffers, **(e.g., see column 7, lines 26-30, elements 111A-111B in Fig. 3)** when the host intends to program the memory device, **(e.g., see column 7, lines 26-30)** the method comprising:"

"transferring data sectors between the host and the large block memory by alternatively using the buffers;" **(e.g., see column 8, lines 1-32; elements 111A-111B, 131-0 AND 131-1 in Fig. 2).** *The host transfers a set of data to BUFA and controller transfers this data to Flash memory. While the controller is writing this data to memory, the host transfers a second set of data to BUFB. After transfer of data from BUFA to memory is complete, the controller transfer the data from BUFB to memory and the host write the third set of data to BUFA. Thus transfer of data between the host and the Flash memory takes place by alternatively using the buffers.*

"issuing a start program command by the controller for programming the large block memory after transferring a number of data sectors with respect to one page;" **(e.g., see column 8, lines 51-60; Fig. 4a-4b).** *For example after transfer of data to BUFA (prior to time t), the controller transfers the data to the memory and begins programming (e.g.,* issuing a start program command) the Flash memory. Although, Conley teaches that the flash memory 131 includes registers (REG 135) for storing pages of data and parallel programming these pages of data to the flash memory, Conley does not teach: "and the large block memory has two buffers therein to serve as a data cache and a page buffer, sending a page of data from the controller to the data cache within the large block memory; after the data cache is full, shifting a data content in the data to page buffer within the large block memory; continuously sending a next page of data to the data cache while a content in the page buffer is programmed to c cell array of the large block memory."

Hosono teaches: "and the large block memory has two buffers therein to serve as a data cache and a page buffer **(e.g., see column 5, lines 26-56; elements 110 and 120 in Fig. 1)**, sending a page of data from the controller to the data cache within the large block memory;" **(e.g., see column 5, lines 26-56; elements 120 and 200 in Fig. 1).** *For example data buffer 200 shown in Fig. 1 is part of the controller which receives data from I/O device and transmits the data to the cache.*

"after the data cache is full, shifting a data content in the data to page buffer within the large block memory;" **(e.g., see column 7, lines 55-56; Figs. 2-3 and 6).** *Flow diagram in Fig. 6 showsthat data from cache is being transferred or shifted from cache to page buffer (see elements CAU and PBU in Fig. 3).*

"continuously sending a next page of data to the data cache while a content in the page buffer is programmed to cell array of the large block memory." **(e.g., see column 14, lines 12-22).** *Disclosures by Conley and Hosono are analogous because both references teach methods of programming non-volatile or flash memory.*

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the pipelined parallel programming taught by Conley to include the cache and page buffer to program and verify the flash memory disclosed by Hosono.

The motivation for using the method to program and verify the flash memory as taught by column 21, lines 15-18 of Hosono is to provide an enhanced erratic program/over-program verifying functionalities.

Therefore, it would have been obvious to combine disclosures by Hosono with Conley to obtain the invention as specified in the claim.

5. In regard to claim 2, Conley teaches:

"wherein the at least two buffers have two buffers, **(e.g., see column 8, lines 1-32; elements 111A-111B**) and the step of transferring data between the host and the large block flash memory comprises:" **(e.g., see column 8, lines 51-60).** *Conley teaches that the buffer is being loaded with pages which inherently consists of a plurality smaller buffers.*

"alternatively using one of the two buffers to store a data transferred from the host;" **(e.g., see column 8, lines 1-32).**

"transferring a previous data stored in the other one of the two buffers to the large block flash memory;" **(e.g., see column 8, lines 1-14).** *After completing transfer of data from BUFA, controller transfers the content of BUFB, which is already transferred from the host. This data is considered previous data.*

"and calculating an address for the data to be programmed to the large block flash memory by the controller, **(e.g., see column 1, lines 50-56)** wherein at least two of the above three different operations can be performed at the same time." **(e.g., see column 8, lines 1-7).** *For example translation of Logical Block Address (LBA) to Logical Block Number (LBN) represents calculating address recited in the claim. Transfer of data from the host to one of the buffers in the controller and the programming of the Flash memory are preformed at the same time.*

6. *In regard to claim 4, Conley teaches:*

"A method of accessing a large block memory of a memory device **(e.g., see column 8, lines 1-14)**, wherein the large block flash memory has a plurality of pages **(e.g., see column 1, line 44)** and each page has a plurality of sectors **(e.g., see column 1, line 46)**, wherein the memory device has a controller to control an access operation between a host and the large block memory of the memory device **(e.g., see column 3, lines 62-67; column 4, lines 1-1-4; elements 101 and 131 in Fig. 2)**, the controller also has two buffers regions," **(e.g., see column 7, lines 26-30, elements 111A-111B in Fig. 3)**

"the method comprising:"

"transferring a portion of a current page data from the host to the controller," **(e.g., see column 8, lines 1-32).** *Although, Conley teaches that the flash memory 131 includes registers (REG 135) for storing pages of data and parallel programming these pages of data to the flash memory, Conley does not teach:* "transferring a portion of the current page data from the controller to a data cache within the large block memory, wherein the two transferring steps can be performed at the same time; shifting the current page data in the data cache to the a page buffer within the large block memory; and programming the current page data into a cell array of the large block memory, and simultaneously performing the foregoing two transferring steps if a next page data is desired to continuously transfer."

Hosono teaches: "transferring a portion of the current page data from the controller to a data cache within the large block memory, wherein the two transferring steps can be performed at the same time;" **(e.g., see column 5, lines 26-56; elements 120 and 200 in Fig. 1).**

"shifting the current page data in the data cache to a page buffer within the large block memory;" **(e.g., see column 7, lines 55-56; Figs. 2-3 and 6).**

"and programming the current page data into a cell array of the large block memory, and simultaneously performing the foregoing two transferring steps if a next page data is desired to continuously transfer." **(e.g., see column 7, lines 55-56; column 14, lines 12-22; Figs. 2-3 and 6).** *For the motivation for combining the two references see the rejection of claim 1 above*

7. *In regard to claim 5, Hosono teaches:*

"wherein "a start program with data cache" command is issued to perform the step of shifting the current page data in the data cache to the page buffer." **(e.g., see column 7, lines 55-56; Fig. 6).** *For example the Fig. 6 (step S2) shows data is transferred or shifted from cache to page buffer.*

8. *In regard to claim 7, Conley teaches:*

"wherein in a time period, at least two of the two transferring steps and the programming step are performed at the same time." **(e.g., see column 8, lines 1-16).** *For example while the controller is transferring data to REG 1, the data already transferred to register is being programmed.*

9. *In regard to claim 8, Conley teaches:*

"wherein in a time period, all of the two transferring steps and the programming step are performed at the same time." **(e.g., see column 9, lines 12-22).** *For example Conley teaches that the transfer of data from the host to the controller and from controller to the one of the register in the memory will overlap with the programming of the flash memory.*

10. *In regard to claim 9, Hosono teaches:*

"wherein when a last page is received, a start program with data cache" command is issued to program the memory cell array." **(e.g., see column 7, lines 55-56; Fig. 6).**

ALLOWABLE SUBJECT MATTER

Claims 6 and 10 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims

1. The primary reason for allowance of claim 6 in instant application is the combination with the inclusion of the following limitation: **wherein the step of shifting the current page data in the data cache to the page buffer is performed when full data of one page is received and a storage space of the page buffer is available.**

2. The primary reason for allowance of claim 10 in instant application is the combination with the inclusion of the following limitation: **wherein before a last page is received, a "start program with data cache" command is issued for simultaneously receiving the data at the data cache and programming the data at page buffer into the cell array of the large block memory.**

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the title of the invention*** *such that it is descriptive of the invention as claimed as required be sec.* ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract*** *should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of* ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Response to Applicant' Remarks

The indicated allowability of some of the claims is withdrawn in view of the newly discovered reference(s). The Examiner apologizes if this will cause any inconvenience. As was stated above the removing of the flash has the effect of adding new matter (e.g., other type memory). There is support in the specification, since the specification clearly specifies invention is related to flash memory (e.g., see description under field of invention and invention summary.

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent No. 6,317,371 to Katayama et al. describes Storage device with an error correction unit and an improved arrangement for accessing and transferring blocks of data stored in a non-volatile semiconductor memory.

2. U. S. Patent No. 6,405,279 to Kondo et al. describes Apparatus and method for controlling rewriting of data into nonvolatile memory.

3. U. S. Patent No. 5,701,516 to Cheng et al. describes High-performance non-volatile RAM protected write cache accelerator system employing DMA and data transferring scheme.

4. U. S. Patent No. 6,684,289 to Gonzalez et al. describes Techniques for operating non-volatile memory systems with data sectors having different sizes than the sizes of the pages and/or blocks of the memory.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF.
HF

2005-12-18

DONALD SPARKS
SUPERVISORY PATENT EXAMINER